The Patent office of the People's Republic Of China

Applicant:. *MATSUSHITA ELECTRIC*	ISSUING DATE:
Agent: *Ma*	
Application No.: *0180 0037*	*2003. 03. 28*
Title: *RADIO RECEIVING DEVICE AND RADIO*	

THE FIRST OFFICE ACTION

1. ☒ The applicant filed a request for substantive examination on Year___Month___Day___ according to Article 35 Paragraph 1 of the Patent Law. The examiner has conducted a substantive examination to the above-mentioned patent application.

   ☐ According to Article 35 paragraph 2 of the Patent Law. Chinese Patent office decided on its own initiative to conduct a substantive examination to the above-mentioned patent application.

2. ☒ The applicant requested to take

   Year *00* Month *1* Day *12* on which an application is filed with the *JP* patent office as the priority date.

   Year_____Month_____Day_____on which an application is filed with the_____patent office as the priority date.

   Year_____Month_____Day_____on which an application is filed with the_____patent office as the priority date.

   ☐ The applicant has submitted the copy of the earliest application document certified by the competent authority of that country.

   ☐ According to Article 30 of the Patent Law, if the applicant has not yet submitted the copy of the earliest application document certified by the competent authority of that country, the declaration for Priority shall be deemed not to have been made.

   ☐ This application is a PCT application.

3. ☐ The applicant submitted the amended document(s) on Year___Month___Day___and Year___Month_____Day after examination, _____submitted on Year_____Month_____Day_____is/are not accepted.

   _____submitted on Year_____Month_____Day_____is/are not accepted

   because the said amendment(s) ☐ is/are not in conformity with Article 33 of the Patent Law.

   ☐ is/are not in conformity with Rule 51 of the Implementing Regulations..

   ☐ The concrete reason(s) for not accepting the amendment(s) is/are presented on the text of Office Action.

4. ☒ The examination has been conducted based on the application text as originally filed.

   ☐ The examination has been conducted based on the following text(s):

   page(s)_____of the specification, Claim(s)_____, and figure(s)_____in the original text of the application submitted on the filing day.

   page(s)_____of the specification, claim(s)_____, and figure(s)_____submitted on Year____Month_____Day____

   page(s)_____of the specification, claim(s)_____, and figure(s)_____submitted on Year____Month_____Day____

5. ☐ This notification was made without undergoing search.

   ☐ This notification was made with undergoing search.

   ☒ The following reference document(s) is/are cited:(the reference numeral(s) thereof will be used in the examination procedure hereafter)

NO.	Reference No. or Title	Publishing Date
1	EP093072 A2	1999, 07 21
2		
3		
4		
5		

6. Concluding comments

☒ on the specification:

- ☐ The contents of the application are in contrary to Article 5 of the Patent Law and therefore are not patentable.
- ☐ The contents of the application do not possess the practical applicability as prescribed in Paragraph 4 of Article 5 of the Patent Law.
- ☐ The specification is not in conformity with the provision of Paragraph 3 of Article 26 of the Patent Law.
- ☒ The presentation of the specification is not in conformity with the provision of Rule 18 of the Implementing Regulations. *and 2 4*

☒ on the claims:

- ☐ Claim(s) _____ belong(s) to non-patentable subject matter as prescribed in Article 25 of the Patent law.
- ☐ Claim(s)_____ do(es) not comply with the definition of a patent as provided in Rule 2 paragraph 1 of the Implementing Regulations.
- ☐ Claim(s)_____ do(es) not possess novelty as requested by Article 22 paragraph 2 of the Patent Law.
- ☒ Claim(s) *1, 7-9* do(es) not possess inventiveness as requested by Article 22 paragraph 3 of the Patent Law.
- ☐ Claim(s)_____ do(es) not possess practical applicability as requested by Article 22 paragraph 4 of the Patent Law.
- ☐ Claim(s)_____ do(es) not comply with the provision of Article 26 paragraph 4 of the Patent Law.
- ☐ Claim(s)_____ do(es) not comply with the provision of Article 31 paragraph 1 of the Patent Law.
- ☒ Claim(s) *1-9* do(es) not comply with provision of Rules 20 to 23 of the Implementing Regulations.
- ☐ Claim(s)_____ do(es) not comply with the provision of Article 9 of the Patent Law.
- ☐ Claim(s)_____ do(es) not comply with the provision of Rule 12 paragraph 1 of the Implementing Regulations.

The detailed analysis for the above concluding comments is presented on the text of this Office Action.

7. Based on the above concluding comments, the examiner is of the opinion that

☐ The applicant should amend the application document(s) in accordance with the requirement as specified in the Office Action.

☒ The applicant should, in his observation, expound the patentability of the application of the application, amend the defects pointed out in the Office Action; or the application can hardly be approved.

☐ The examined deems that the application lacks substantive features to make it patentable. Therefore, the application will be rejected if no convincing reasons are provided to prove its patentability.

8. The applicant should pay attention to the following matters:

(1) According to Article 37 of the Patent Law, the applicant is required to submit his observations within **Four** months upon receipt of this Office Action. If the time limit for making response is not met without any justified reason, the application to have been withdraw.

(2) The amendment(s) made by the applicant must meet the requirements of Article 33 of the Patent Law. The amended text should be in duplicate, its format should conform to the related confinement in the Guidance for Examination.

(3) The applicant and/or the agent should not go to the Chinese Patent Office to interview the examiner without being invited.

(4) The observation and/of the amended document(s) must be mailed of delivered to the Receiving Section of the Chinese Patent Office. No legal effect shall apply for any document(s) that not mailed to or reached the Receiving Section.

9. The text of this Office Action contains ___2___ page(s), and has the following attachment(s):

☒ ___1___ copies of the cited references, all together ___2-3___ pages.

☐

Examination Dept. No._____ Examiner_____ Seal of Examination Dept. for business only _____.

(if the Office Action wasn' t stamped by the specified seal, it has no legal effect)

EUROPEAN PATENT APPLICATION

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(54) CDMA multiuser receiver featuring a combination of array antenna and multiuser interference cancellers

(57)   In order to effectively reduce a size of a CDMA multiuser receiver while maintaining an excellent interference cancellation, an array antenna is combined with a multiuser receiver. The multiuser receiver includes signal processing means which is supplied with incoming signals received at the array antenna. The signal processing means estimates interfering signals with respect to each of the antenna elements and with respect to each of simultaneously accessing users.
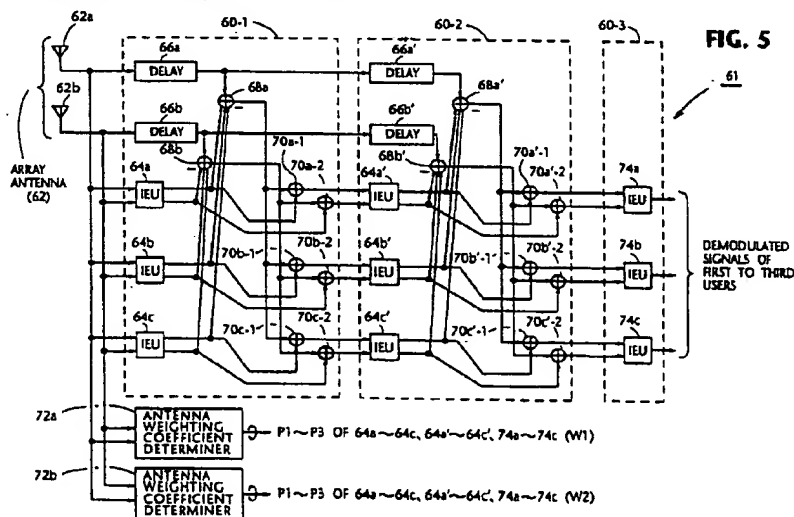
FIG. 5

EP 0 930 727 A2

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001]   The present invention relates to a CDMA (code-division multiple-access) multiuser receiver which combines directivity control of an array antenna and interference canceling operations. The CDMA multiuser receiver according to the present invention features a small size and excellent interference cancellation. By way of example, the present invention may be applicable to the receiver installed in the base station of a cellular mobile communications system.

2. Description of the Related Art

[0002]   It is expected that CDMA is able to markedly increase a subscriber's capacity and thus find an extensive application in a cellular mobile communications system (for example). However, the mobile communications utilizing CDMA (viz., spread-spectrum) techniques have suffered, at a receiver side, the problems of interference caused by delayed signal due to multiple transmission paths and concurrently communicating other party's signals.

[0003]   As is known in the art, an array antenna is able to suppress and cancel interference through directivity control. On the other hand, a multiuser receiver is a receiver which demodulates all the user's signals by implementing mutual interference cancellation using all the user's spreading codes and channel characteristics. The multiuser receiver itself is known in the art. One example of such a receiver is disclosed in a paper by M. K. Varanasi and B. Aazhang, entitled "Multistage Detection in Asynchronous Code-Division Multiple-Access Communications"; IEEE Transactions on Communications, Vol. 38, No. 4, April 1990, pp. 509-519 (Prior Paper 1). Other example of a conventional multiuser receiver is disclosed in a paper by M. Sawahashi, et al., entitled "Serial Canceler Using Recursive Channel Estimation by Pilot Symbols for DS-CDMA", Electronics Information Communications Association of Japan, Technical Report RCS95-50, July 1995 (Prior Paper 2).

[0004]   According to the apparatus disclosed in the aforesaid Prior Paper 1, all the user's signals are demodulated at an initial stage of the apparatus, after which an interfering replica of each user is produced. Subsequently, interference cancellation is implemented by reducing an interference replica of each of the users other than a desired user from a received signal. At the next stage, the signal, which has been obtained through the interference cancellation, is again demodulated in connection with the desired (intended) user and therefore, the signal quality of the demodulation result at the second stage is higher than that at the first stage. Thus, the conventional technique, disclosed in Prior Paper 1,

is to improve the interference cancellation by repeating a series of signal processes using multi-stage configuration.

[0005]   Channel estimation is necessary to demodulate the signal of each user and produce an interference replica. The aforesaid Prior Paper 2 discloses that a channel (viz., transmission path) is recursively estimated at each stage thereby to prevent deterioration of the interference cancellation characteristics due to channel estimation error.

[0006]   Another example of the multiuser receiver is disclosed in a paper by Yoshida and Ushirokawa, entitled "CDMA Multi-Stage Interference Canceler with Recursive Channel Estimation Based on Symbol Replica Processing", the Institute of Electronics, Information and Communication Engineers, Technical Report of IEICE, A. p96-157, EMCJ96-92, RCS96-171, February 1997 (Prior Paper 3).

[0007]   The above-mentioned Prior Paper 3 discloses a multi-stage type CDMA multiuser receiver. According to this known technique, the size of the apparatus can be reduced through the use of symbol replica processing. At the same time, it is possible to realize interference cancellation at the unit of multi-path in the case of implementing recursive channel estimation thereby to improve interference cancellation in the case of multi-path transmission.

[0008]   Fig. 1 is a drawing showing a CDMA multiuser receiver that is based on the known techniques disclosed in Prior Paper 3. The CDMA multiuser receiver of Fig. 1 is comprised of three-stage interference cancelers 10-1 to 10-3. At the first two stages of interference cancelers 10-1 and 10-2, the signals of all the users, the number of which is assumed three, are demodulated and then subjected to interference cancellation. That is, this means that the multiuser interference cancellation is implemented.

[0009]   As shown in Fig. 1, the interference canceler 10-1 at the first stage is provided with a delay unit 12, three IEUs (interference estimation units) 14a-14c, an adder 16, and another adders 18a-18c. The interference canceler 10-2 is configured in the same manner as the canceler 10-1 and is comprised of three IEUs (interference estimation units) 14a'-14c', an adder 16', and another adders 18a'-18c'.

[0010]   On the other hand, the interference canceler 10-3 at the final stage is provided with IEUs 20a-20c each of which differs from those provided at the first and second stages.

[0011]   A received signal is directly applied to the first stage (viz., interference canceler 10-1). The interference canceler 10-3 at the final stage is not provided with any delay unit and any adder. The IEUs 20a-20c generate demodulated signals respectively corresponding to the first to third users.

[0012]   The operations of the interference cancelers 10-1 and 10-2, which are respectively provided at the first and second stages, are identical with each other

and thus, there will be described the operation of the first stage. The three IEUs 14a-14c respectively output estimated interference spread signals that are applied to the adder 16. The delay unit 12 operates such as to delay the incoming signal by the time for which each of the IEUs 14a-14c estimates the interference and outputs the result thereof, and applies the output thereof to the adder 16 and the delay unit 12' of the second stage. The adder 16 subtracts the outputs of the IEUs 14a-14c from the output of the delay unit 12, and applies the output thereof to the adders 18a-18c that are respectively assigned to the users. Each of the adders 18a-18c sums the output of the adder 16 and the output of the corresponding IEU (14a, 14b, or 14c), and applies the resultant sum to the second stage.

[0013]   The IEUs 14a-14c of the first stage and the IEUs 14'a-4c' of the second stage are substantially identical with each other in terms of configuration as well as operations, and accordingly there will be described only the IEU 14a of the first stage.

[0014]   The IEU 14a of Fig. 2 is configured under the assumption that the number of paths of the incoming signal is three (3). In the drawing, the circuits prepared for first to third propagation paths are depicted by P1-P3. Since the circuits for the multiple paths are identical with each other, the description is made with reference to the circuit P1 for the first path. The IEU shown in the drawing is generally comprised of a front section (stage) S1, an intermediate section S2, and a rear section S3. More specifically, the front section S1 comprises a spread-spectrum despreader 22 and a detector 24, while the intermediate section S2 comprises an adder 25 and a discriminator 26. Finally, the rear section S3 comprises a multiplier 27, a spread-spectrum modulator 28 and an adder 29. Further, the detector 24 comprises a channel estimator 24a, a complex conjugate generator 24b, and a multiplier 24c.

[0015]   The received signal (incoming signal) is split and applied to the circuits P1-P3 prepared for the three transmission paths. The despreader 22 despreads the incoming signal using the first user's spreading code at the timing in synchronism with the spreading code transmitted via the first path, and outputs the operation result.

[0016]   The detector 24 is supplied with the output of the despreader 22, implementing channel estimation at the channel estimator 24a, applying the estimated channel characteristics to the multiplier 24c via the complex conjugate generator 24b, and implementing carrier phase coherent detection. The multiplier 24c implements amplitude weighting on the output of the despreader 22, using the output of the complex conjugate generator 24b, for the purpose of Rake combination at the subsequent block. The amplitude weighting is for implementing Rake combination (maximum ratio combination) on the output of the despreader 22.

[0017]   It is deemed advantageous to operate the detector 24, in an environment of fading, using coherent

detecting techniques which are disclosed in Prior Paper 2 and via which a carrier is estimated through the use of pilot symbols inserted on a time axis.

[0018]   The adder 25 combines, using Rake combination techniques, the weighted outputs of the multipliers 24c respectively provided in the circuits P1-P3 for the three paths. The combined signal is fed to the discriminator 26 that determines the most likely transmitted symbol.

[0019]   The output of the discriminator 26 is again split and applied to circuits P1-P3 of the third section S3, which are respectively assigned to the three transmission paths. The multiplier 27 multiplies the output of the discriminator 26 with the estimated channel characteristics, viz., the output of the channel estimator 24a. A spread-spectrum modulator 28 spreads the output of the multiplier 27 using the first user's spreading code at the timing which is in synchronism with the spreading code transmitted via the first path.

[0020]   An adder 29 sums (synthesizes) the outputs of the circuits P1-P3 which are respectively assigned to the three paths and which are the replicas of respective paths. Thus, an interference replica of the first user is generated.

[0021]   The interference canceler 10-3 shown in Fig. 1 is comprised of IEUs 20a-20c which are configured in a manner identical with each other, and accordingly, only the IEU20a provided for the first user will be described.

[0022]   Referring to Fig. 3, there is shown the IEU 20a in block diagram form. As shown in Fig. 3, the IEU 20a is configured in a manner exactly identical with those of the front and intermediate sections shown in Fig. 2. Therefore, the reference numerals already used for the blocks of Fig. 2 are attached to the counterparts of Fig. 3 and the description thereof will be omitted.

[0023]   On the other hand, the techniques for canceling signal interference by applying an array antenna to a CDMA's single user receiver is disclosed in a paper by R. Kohno, H. Imai, M. Hatori and S. Pasupathy, entitled "Combination of an Adaptive Array Antenna and a Canceler of Interference for Direct-Sequence Spread-Spectrum Multiple-Access System", IEEE Journal on selected areas in communications, Vol. 8, N. 4, May 1990, pp. 675-682 (Prior Paper 4).

[0024]   According to the apparatus disclosed in the aforesaid Prior Paper 4, the array antenna is controlled such as to be directed to an arrival angle of a desired signal and acquires the same, after which the interfering signal components within the directivity are despread. The apparatus demodulates the signal components and generates a temporal symbol, after which the apparatus again spreads the signal and generates interfering signal components. In other words, the apparatus carries out interference cancellation by subtracting the interfering signal components from the signal received by the array antenna, and then demodulates the desired (intended) user's signal. Although this conventional apparatus utilizes spreading codes and channel charac-

teristics of all users, it is understood that the apparatus implements interference cancellation for a single user and thus is classified as a single user receiver.

[0025]   Fig. 4 shows one example of the above-mentioned conventional receiver wherein an array antenna 30 is combined with an interference canceler. In order to simplify the description and the drawing, it is assumed that an array antenna consists of two antenna elements and the number of total users is three. The receiver is a single user DCMA receiver for demodulating one user (the third user in this particular case).

[0026]   Superimposed data of desired and interfering signals are applied to two antenna elements 30a and 30b. The signal received at the antenna elements 30a and 30b are respectively weighted, at corresponding complex multipliers 32a and 32b, by antenna weighting coefficients W1 and W2 and thereafter added at an adder 34. The output of the adder 34 is applied to despreader 36a and 36b which are provided for the two users (viz., first and second users) other than the third user (whose signal is to be received in the instant case). Further, the output of the adder 34 is also applied to a delay unit 38. The outputs of the despreader 36a and 36b are respectively applied to discriminators 40a and 40b at which temporal symbol discrimination is implemented. The outputs of the discriminators 40a and 40b (viz., signals representative of temporal symbols) are respectively applied to spreader 42a and 42b which issues interfering signal components based on the discrimination results.

[0027]   A delay unit 38 is used to delay the output of the adder 34, which is denoted by 34a and is to be applied to an adder 44. In more specific terms, the delay unit 38 is provided to delay the signal 34a (viz., the output of the adder 34) until a signal 34b, applied to the despreaders 36a and 36b, is outputted from spreaders 42a and 42b.

[0028]   The adder 44 subtracts the outputs of the spreaders 42a and 42b (viz., interfering signal components) from the output of the delay unit 38, and applies the result to a despreader 46 and a delay unit 48.

[0029]   The output of the despreader 46 is applied to a discriminator 50 which demodulates the signal of the third user and outputs the demodulated signal to an external circuit (not shown). That is, the despreader 46 and the discriminator 50 are provided for the third user. On the other hand, the output of the discriminator 50 is also applied to a spreader 52 for the third user, via which a spread signal for the third user is obtained.

[0030]   The delay unit 48 is to delay the output of the adder 44 (depicted by 44b) by a time period for which the output of the adder 44 (depicted by 44a) has been subjected to symbol discrimination and the spreader 52 generates the spread signal for the third user. The signal thus delayed is applied to the adder 54.

[0031]   The adder 54 produces an error signal 56 by subtracting the output of the spreader 52 from the output of the delay unit 48. The error signal 56 is fed to an

antenna weighting coefficient determiner (adaptively renewing means) 58. This determiner 58 controls the directivity of the array antenna 30 using the signals received at the antenna elements 30a and 30b along with known adaptive algorithm.

[0032]   The receiver shown in Fig. 4 is an apparatus for use in producing the demodulated signal only for the third user. In other words, in order to demodulate the signals of the other users, viz., first and second users, it is necessary to provide the receivers respectively dedicated to the first and second users.

[0033]   There has been so far no proposal of combining an array antenna and a CDMA multiuser receiver. By way of example, if an array antenna is simply applied to the multiuser receivers shown in Figs. 1-3, particularly the interference estimating section becomes complex thereby to be unable to simplify the overall configuration of the receiver.

[0034]   In addition, the single user receiver shown in Fig. 4, which features a combination of an array antenna and an interference canceler, suffers from the following problem when applied to the case of simultaneously processing a plurality of users. That is, in such a case, it is absolutely necessary to prepare a plurality of identical receivers that are arranged in parallel for respective users.

SUMMARY OF THE INVENTION

[0035]   Accordingly, the object of the present is to provide a CDMA multiuser receiver which is able to demodulate a plurality of user's signals, without incurring increase in the arrangement or size, by combining an array antenna and a multiuser receiver.

[0036]   Another object of the present invention is to provide a CDMA multiuser receiver which is based on an effective combination of an array antenna and an interference canceler and features the marked reduction of size of the apparatus with excellent interference cancellation.

[0037]   In brief, these objects are achieved by techniques wherein in order to effectively reduce a size of a CDMA multiuser receiver while maintaining an excellent interference cancellation, an array antenna is combined with a multiuser receiver coupled to said array antenna. The multiuser receiver includes signal processing means which is supplied with incoming signals received at said array antenna. The signal processing means estimates interfering signals with respect to each of the antenna elements and with respect to each of simultaneously accessing users.

BRIEF DESCRIPTION OF THE DRAWIINGS

[0038]   The features and advantages of the present invention will become more clearly appreciated from the following description taken in conjunction with the accompanying drawings in which like elements are

denoted by like reference numerals and in which:

Fig. 1 is a diagram schematically showing a conventional CDMA receiver in block diagram, having referred to in the preceding paragraphs;

Fig. 2 is a diagram sowing in detail an interference estimation unit (IEU) of Fig. 1;

Fig. 3 is a diagram sowing in detail another IEU of Fig. 1;

Fig. 4 is a diagram schematically showing another conventional CDMA receiver in block diagram, having referred to in the preceding paragraphs;

Fig. 5 is a diagram schematically showing a CDMA receiver according to a first embodiment of the present invention;

Figs. 6 to 8 are each diagrams showing a detailed arrangement of a block of Fig. 5;

Fig. 9 is a diagram schematically showing a CDMA receiver according to a second embodiment of the present invention;

Figs. 10 to 12 are each diagrams showing a detailed arrangement of a block of Fig. 9;

Fig. 13 is a diagram schematically showing a CDMA receiver according to a third embodiment of the present invention; and

Figs. 14 and 15 are each diagrams showing a detailed arrangement of a block of Fig. 13.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0039]   Referring now to Fig. 5, a CDMA multiuser receiver 61 according to a first embodiment of the present invention is schematically shown in block diagram form. Figs. 6-8 illustrate detailed arrangements of IEUs 64a, 64a', and 74a of Fig. 5, respectively. Incoming signals are received at an array antenna 62 that comprises two antenna elements 62a and 62b in this particular embodiment. It is assumed that the number of multiple transmission paths is three, the number of stages for interference cancellation is three, and the number of simultaneously accessing users is three. It is to be noted that the aforesaid numbers of antenna elements, multiple transmission paths, etc. are exemplary and in no way limited thereto.

[0040]   The receiver shown in Fig. 5 comprises three interference cancelers 60-1 to 60-3, among which the interference cancelers 60-1 and 60-2 are configured in exactly the same manner except for the connection of the outputs of delay units.

[0041]   As shown, the interference canceler 60-1 is comprised of three IEUs 64a to 64c which are respectively provided for first to third users, two delay units 66a and 66b whose number is the same as that of the antenna elements 62a and 62b, two adders 68a and 68b whose number is also identical with that of the antenna elements, and six (="the number of users" × "the number of antenna elements") adders 70a-1 and

70a-2, 70b-1 and 70b-2, and 70c-1 and 70c-2.

[0042]   As mentioned above, the interference canceler 60-2 is configured in the same manner as the canceler 60-1, and therefore the counterparts of the canceler 60-2 are depicted by like numerals with a prime. That is, the interference canceler 60-2 of the second stage is comprised of three IEUs (interference estimation unit) 64a' to 64c' which respectively correspond to the first to third users, two delay units 66a' and 66b' the number of which is identical with that of the antennas, two adders 68a' and 68b' the number of which are also identical with that of the antenna, and six (="the number of users" × "the number of antennas") adders respectively depicted by 70a'-1 and 70a'-2, 70b'-1 and 70b'-2, and 70c'-1 and 70c'-2.

[0043]   Since the IEUs 64a to 64c are identical with each other in terms of configuration as well as operation, the IEU 64a will mainly be described for the sake of simplifying the disclosure. The IEU 64a is supplied with the signals received at the antenna elements 62a and 62b, and generates two spread "interference estimating signals" which respectively correspond to the antenna elements 62a and 62b. As shown, the outputs of the IEU 64a are applied to adders 68a and 68b, and adders 70a-1 and 70b-2. Each of delay units 66a and 66b is to delay the signal applied thereto until each of the IEUs 64a to 64c produces the output thereof. The output of the delay 66a is applied to the adder 68a and a delay unit 68a' of the next stage 60-2, and similarly, the output of the delay 66b is fed to the adder 68b and a delay unit 68b' of the next stage 60-2.

[0044]   By the way, if the first interference canceler 60-1 is able to completely or sufficiently remove interference of one user against the other, there is no need for providing the following canceler 60-2. However, such interference can not be rejected using a signal canceler and thus, it may be typical to provide one or two canceling stages prior to the final stage.

[0045]   The adder 68a subtracts the outputs of IEUs 64a to 64c, which correspond to the antenna element 62a, from the output of the delay unit 66a. The adder 70a-1 adds the subtraction result outputted from the adder 68a and one of the outputs of the IEU 64a, which corresponds to the antenna element 62a. As mentioned later, each of the two outputs of the IEU 64a is a spread signal. In a similar manner, the adder 68b subtracts the outputs of IEUs 64a to 64c, which correspond to the antenna element 62b, from the output of the delay unit 66b. The adder 70b-1 adds the subtraction result outputted from the adder 68b and the other output of the IEU 64a, which corresponds to the antenna element 62b.

[0046]   It is understood that the IEU 64a', included in the second interference canceler 60-2, is supplied with a signal which includes the interfering components relating to only the first user (although ideal).

[0047]   Antenna weighting coefficient determiners 72a and 72b are supplied with the incoming signals received

at the antenna elements 62a and 62b, and respectively generate outputs W1 and W2 which are applied to circuits P1 to P3 of each of the IEU, 64a-64c, 64a'-64c', and 74a-74c.

[0048]   The IEU 64a of the interference canceler 60-1 will be described in detail with reference to Figs. 5 and 6. The IEU 64a comprises three circuits P1 to P3 which are respectively provided for three transmission paths. In other words, the IEU 64a is configured so as to comply with the case in which the number of multiple transmission paths is three. Since the circuits P1 to P3 are substantially identical with each other, only the circuit P1 is described below. As shown in Fig. 6, IEU 64a is generally comprised of a first section S1, a second section S2, and a final section S3. The section S1 comprises two spread-spectrum despreaders (denoted by "despreading" in the drawing) 80a and 80b, whose number equals that of the antenna elements 62a and 62b. The section S1 further comprises multipliers 82a and 82b, an adder 84, and a detector 86. The first section S1 is coupled to the final section S3 by way of an adder 88 and a discriminator 90 (viz., section S2) each of which is common to all the circuits P1 to P3.

[0049]   As shown in Fig. 6, a first circuit P1 of the final section S3 comprises a multiplier 92, multipliers 94a and 94b whose number equals that of the antenna elements, spread-spectrum despreaders 96a and 96b, adders 98a and 98b, and multipliers 100a and 100b. Each of the adders 98a and 98b is provided so as to add the outputs generated from the circuit P1 to P3 of the section S3. Subsequently, the outputs of the adders 98a and 98b are respectively multiplied, at the multiplier 100, by a weighting coefficient α having a value less than unity, and then applied to the following section.

[0050]   The detector 86 of the first section S1 comprises a channel estimator 86a, a complex conjugate generator 86b, and an adder 86c. The spread-spectrum despreaders 80a and 80b operate such as to despread the incoming signals using a despreading (viz., spreading) code previously assigned to the first user, in which the despreading code is correctly phased (synchronized) with the spreading code transmitted via the first propagation path. The multipliers 82 and 82b respectively multiply the outputs of the despreaders 80a and 80b by antenna weighting coefficients W1 and W2, and apply the multiplication results to the adder 84. As mentioned above, the coefficients W1 and W2 are generated from the antenna weighting coefficient determiners 72a and 72b (Fig. 5).

[0051]   The detector 86 operates in exactly the same manner as the conventional detector 24 of Fig. 2. As mentioned above, the multiplier 86c weights the output of the adder 64 using the output of the complex conjugate generator 86b in order to prepare for Rake combination (viz., maximum ratio combination) at the adder 88. That is the adder 88 receives the outputs from the circuits P1 to P3 which are assigned to three different transmission paths, and carries out Rake combination.

The signal combined at the adder 88 is fed to the discriminator 90 at which most likely transmitted symbols are determined.

[0052]   The multiplier 92 of the section S3 multiplies the output of the discriminator 90 by the output of the channel estimator 86a in order to estimate an interference replica. This operation is implemented at each of the circuits P1 to P3. The estimated interference replica (viz., output of the multiplier 92) is then split into two (viz., the number of antenna elements employed) which are applied to the multipliers 94a and 94b. As shown, the multipliers 94a and 94b multiply the outputs of the multiplier 92 by complex conjugates W1* and W2* which are respectively generated by complex conjugate generators 77a and 77b using the aforesaid antenna weighting coefficients W1 and W2. The outputs of the multipliers 94a and 94b are respectively applied to spread-spectrum modulators 96a and 96b and are spread thereat in a manner to be correctly phased (synchronized) with the spreading code transmitted via the first propagation path. More specifically, the modulators 96a and 96b spread respectively the estimated interfering replicas in connection with the antenna elements 62a and 62b.

[0053]   Adders 98a and 98b respectively add the spread signals issued from the modulators 96a and 96b in each of the circuits P1 to P3. Thus, the adders 98a and 98b output, respectively, the spread signals indicative of the estimated interference replicas regarding the antenna elements 62 and 62b. The following multipliers 100a and 100b multiply respectively the outputs of the adders 98a and 98b by a weighting coefficient α with a value less than unity, and apply the multiplication results to the following section. The coefficient α is able to suppress "emphasized interference" due to a channel estimation error(s) thereby to improve the interference cancellation characteristics, which is disclosed in detail in the aforesaid Prior Paper 4.

[0054]   If the antenna weighting coefficient utilizes a complex conjugate vector relating to a steering vector which is determined depending on signal's arrival angles and which indicates phase difference between antenna elements, the signal obtained by antenna weight composition (viz., antenna weighting coefficients) is an in-phase composed signal. In this case, it is possible to correctly reproduce the interference of each antenna element using the steering vector and the signal weighted by antenna coefficients. Further, if the interference cancellation is implemented with each antenna before the antenna weighting is carried out with each user, it is possible to effectively combine the antenna directivity control and a plurality of interference cancelers.

[0055]   Antenna weighting coefficients are able to be generated using conventional techniques. For further details thereof, reference should be made, for example, to a paper by R.O. Schmidt, et al., entitled "Multiple Emitter Location and Signal Parameter Estimation",

IEEE Trans., Vol. AP-34, No. 3, pp. 276-286, March 1986, or a paper by R. Roy and T. Kailath, entitled "ESPRIT-Estimation of signal Parameters via Rotational Invariance Techniques", IEEE Trans., Vol. ASSP-37, pp. 984-995, July 1989.

[0056]   As shown in Fig. 5, the antenna weighting coefficient determiner 72a outputs nine independent coefficients that are applied to three IEUs of each of the interference canceling stages 60-1 to 60-3. However, if the antenna weighting coefficients are successively renewed, the coefficients are generated, only for the first stage 60-1, using an error between the demodulated result and the known symbol. In this case, it is possible that the stages following the first stage is able to utilize the same antenna weighting coefficients as those used in the first stage.

[0057]   Fig. 7 is a block diagram showing the details of the IEU 64a' that is configured in the same manner as that of the IEU 64a of Fig. 6, and thus, the further descriptions of Fig. 7 will be omitted for the sake of simplifying the disclosure.

[0058]   Fig. 8 is a block diagram showing the details of the IEU 74a. As shown, the IEU 74a comprises two sections that are respectively identical with the sections S1 and S2 of Fig. 6 or 7, and thus are labeled S1 and S2.

[0059]   A second embodiment will be described with reference to Figs. 9, 10, 11 and 12 which respectively correspond to Figs. 5, 6, 7 and 8 of the first embodiment. In connection with the second embodiment, it is assumed, as in the first embodiment, that the number of multiple transmission paths is three, the number of stages for interference cancellation is three, and the number of simultaneously accessing users is three. It is to be noted that the aforesaid numbers of antenna elements, multiple transmission paths, etc. are exemplary and in no way limited thereto.

[0060]   The second embodiment differs from the first embodiment, in terms of arrangement, as listed below:

(1) IEUs provided in the first stage 60-1 of Fig. 9 are differently configured compared with the counterparts of the first stage of Fig. 5 and therefore are denoted by 63a, 63b, and 63c in Fig. 9;

(2) IEUs provided in the second stage 60-2 of Fig. 9 are differently configured compared with the counterparts of the second stage of Fig. 5 and therefore are denoted by 63a', 63b', and 63c' in Fig. 9;

(3) IEUs provided in the third stage 60-3 of Fig. 9 are differently configured compared with the counterparts of the third stage of Fig. 5 and therefore are denoted by 73a, 73b, and 73c in Fig. 9;

(4) the first stage 60-1 of Fig. 9 lacks the adders 70a-1, 70a-2, ..., 70c-1 that are provided in the first stage of Fig. 5; and

(5) the second stage 60-2 of Fig. 9 lacks the adders 70a'-1, 70a'-2, ..., 70c'-1 that are provided in the second stage of Fig. 5.

[0061]   Fig. 10 shows the details of the IEU 63a (Fig. 9) in which the output of the multiplier 92 of each of the circuits P1 to P3 is directly applied to the IEU 63a' of the next stage 60-2. Other than this, the IEU 63a is configured in a manner that is identical with the corresponding IEU 64a of the first embodiment. Since the output of the multiplier 92 of the circuit P1 is the estimated signal of the first user itself, it is understood that the first interference canceler 60-1 of the second embodiment requires no longer the adders 70a-1, 70a-2, ..., 70c-1, and 70c-2 of the IEU 64a of the first embodiment.

[0062]   In order to comply with the above-mentioned modification of the IEU 63a, the IEU 63a' of the second interference canceler 60-2 has the first section S1 which includes an adder 85 in addition to the functional blocks already discussed with the first embodiment. The adder 85 is to add the estimated signal of the first user (in the illustrated case of Fig. 11) to the output of the adder 84. The section S3 of the IEU 63a' is identical with the second 3 of the IEU 63a and hence, the description thereof will be omitted for the sake of simplifying the disclosure.

[0063]   Fig. 12 is a block diagram showing the details of the IEU 73a of Fig. 9. The IEU 73a is identical, in terms of configuration, with a combination of the first and second sections S1 and S2 of Fig. 10 or 11 and accordingly, further description thereof will not been given for brevity.

[0064]   A third embodiment of the present invention will be described with reference to Fig. 13, 14 and 15 that correspond respectively to Figs. 9 and 11 of the second embodiment. In connection with the third embodiment, it is assumed, as in each of the preceding embodiments, that the number of multiple transmission paths is three, the number of stages for interference cancellation is three, and the number of simultaneously accessing users is three. It is to be noted that the aforesaid numbers of antenna elements, multiple transmission paths, etc. are exemplary and in no way limited thereto.

[0065]   Fig. 13 shows that the outputs of delay units 66a and 66b are not directly applied to the delay units 66a' and 66b', instead of which the outputs of the adders 68a and 68b are respectively applied to the delay units 66a' and 66b'. That is, the first interference canceler 60-1 applies the error signals, produced from the adders 68a and 68b, to the delay units 66a' and 66b', and IEUs 65a', 65b', and 65c'. In order to meet this modification, each of IEUs 65a' to 65c' of the second stage 60-2 is slightly changed in the configuration thereof as shown in Fig. 14. On the other hand, the IEUs (denoted by 65a to 65c) of the first stage 60-1 are configured in exactly the same as the counterparts 63a to 63c. However, the IEU 65a is shown in Fig. 15 for the convenience of describing the disclosure. IEUs 75a to 75c of the third stage 60-3 are identical with each other and respectively identical with the IEUs 73a to 73c, and accordingly the drawing of the IEU 75a (for example) is not presented for simplifying the disclosure.

[0066]   As shown in Figs. 13, 14 and 15, the third sec-

tion S3 of the IEU 65a' is provided with an adder 93 to which the outputs of the multipliers 92 of the IEU 65a (Fig. 14) are directly applied. As mentioned above, according to the third embodiment, the error signals from the adders 68a and 68b are directly applied to the second interference canceler 60-2. This implies that the third embodiment is able to reduce a memory capacity compared with the second embodiment.

[0067]   It will be understood that the above disclosure is representative of only three possible embodiments of the present invention and that the concept on which the invention is based is not specifically limited thereto.

Claims

1. A CDMA (code division multiple access) multiuser receiver comprising:

    an array antenna including a plurality of antenna elements; and
    a multiuser receiver coupled to said array antenna, said multiuser receiver including signal processing means which is supplied with signals from said array antenna, said signal processing means estimating interfering signals with respect to each of said plurality of antenna elements and with respect to each of simultaneously accessing users.

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FIG. 1
(PRIOR ART)

DEMODULATED
SIGNALS OF
FIRST TO THIRD
USERS

INTERFERENCE
CANCELER
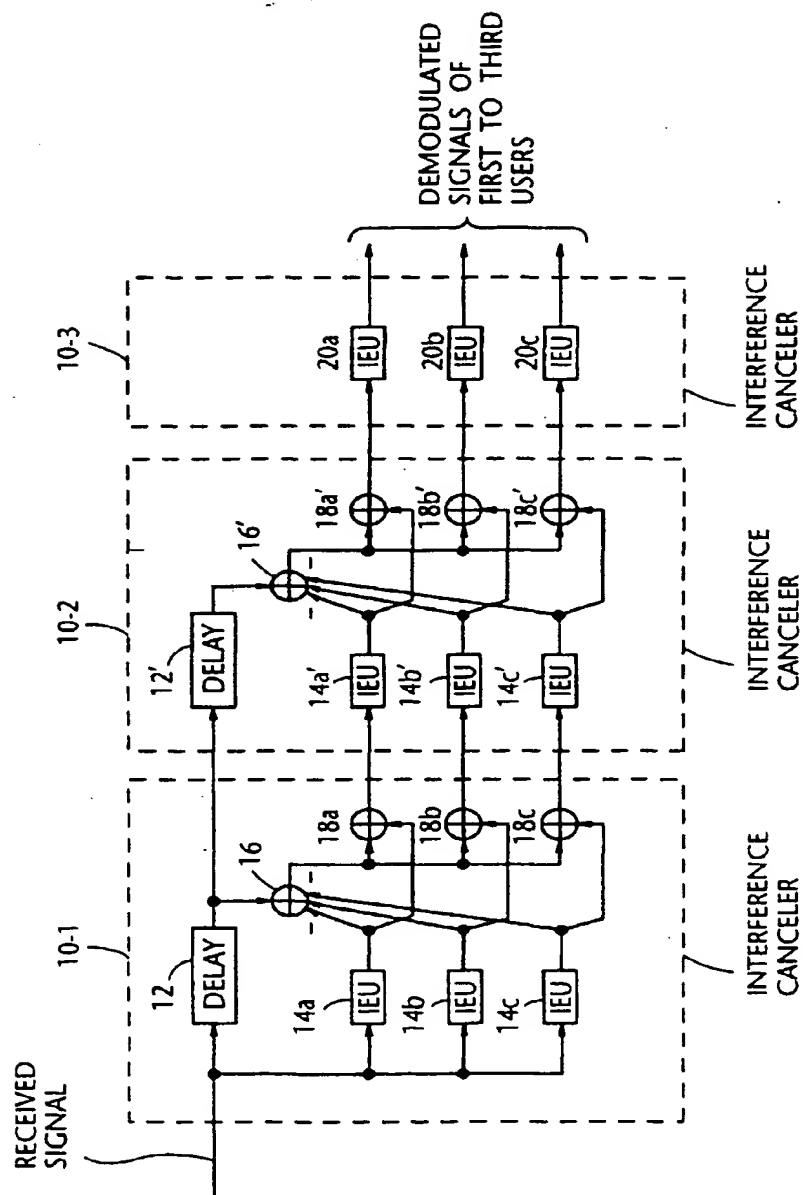
FIG. 2
(PRIOR ART)

FIG. 3
(PRIOR ART)

IEU 20a

DE-SPREADING

22

P1   P2   P3

24a   24b   24c

CHANNEL ESTIMATE

COMPLEX CONJUGATE GENERATOR

24

25   26

DISCRIMINATOR

DEMODULATED SIGNAL OF FIRST USER

18a'

11

FIG. 4
(PRIOR ART)

FIG. 5

61

DEMODULATED SIGNALS OF FIRST TO THIRD USERS
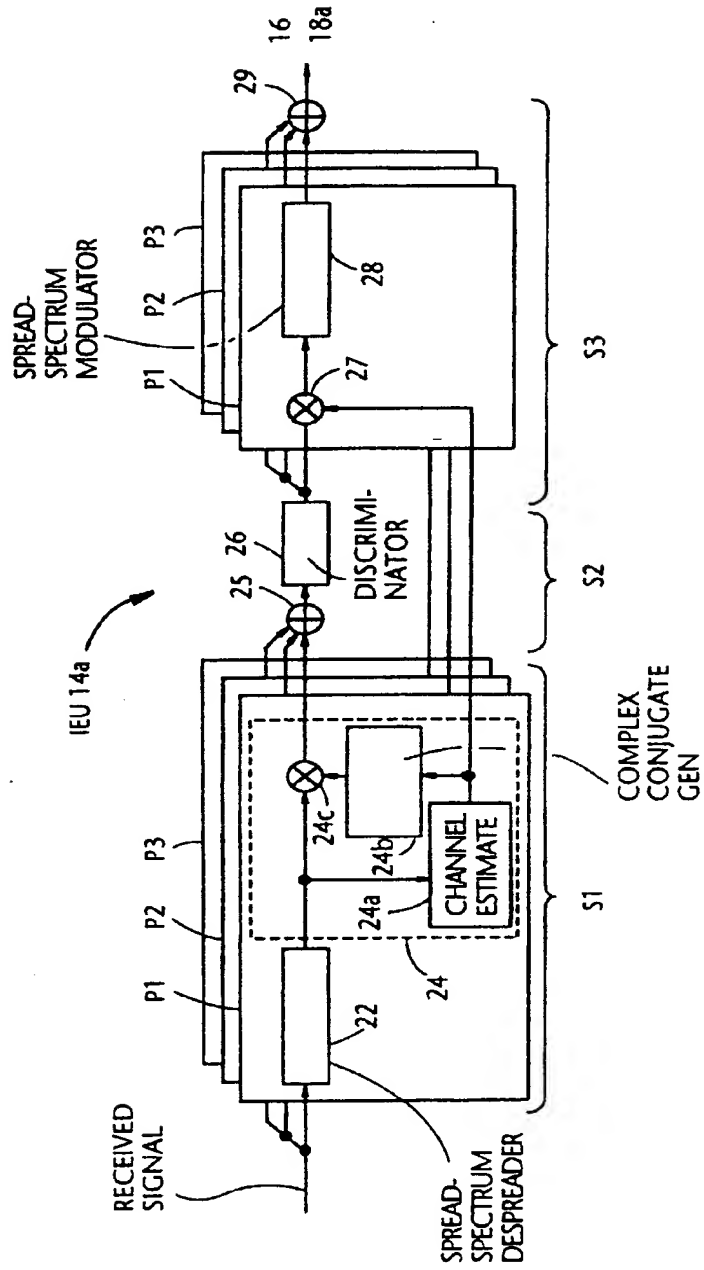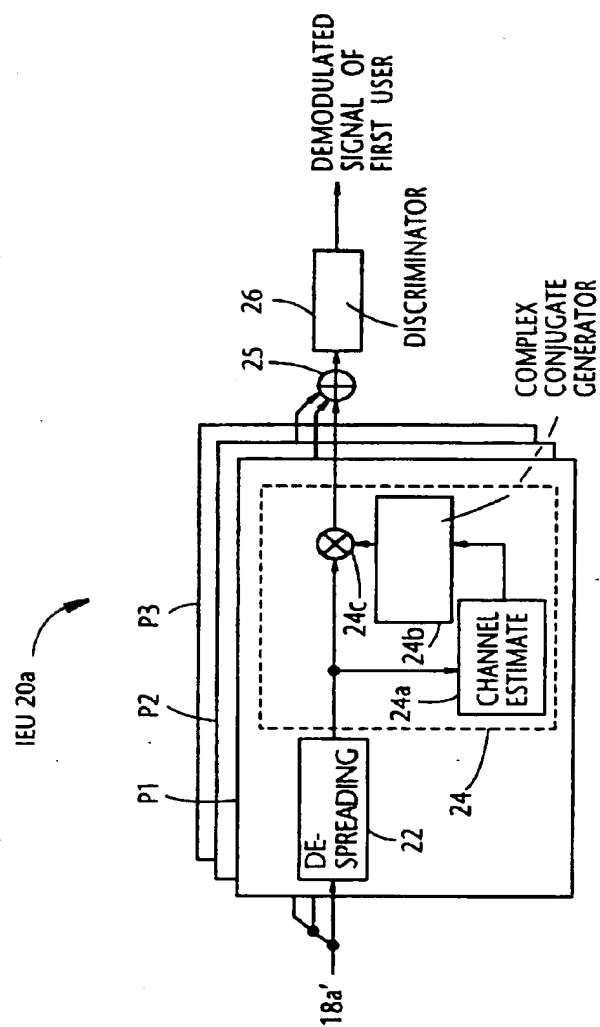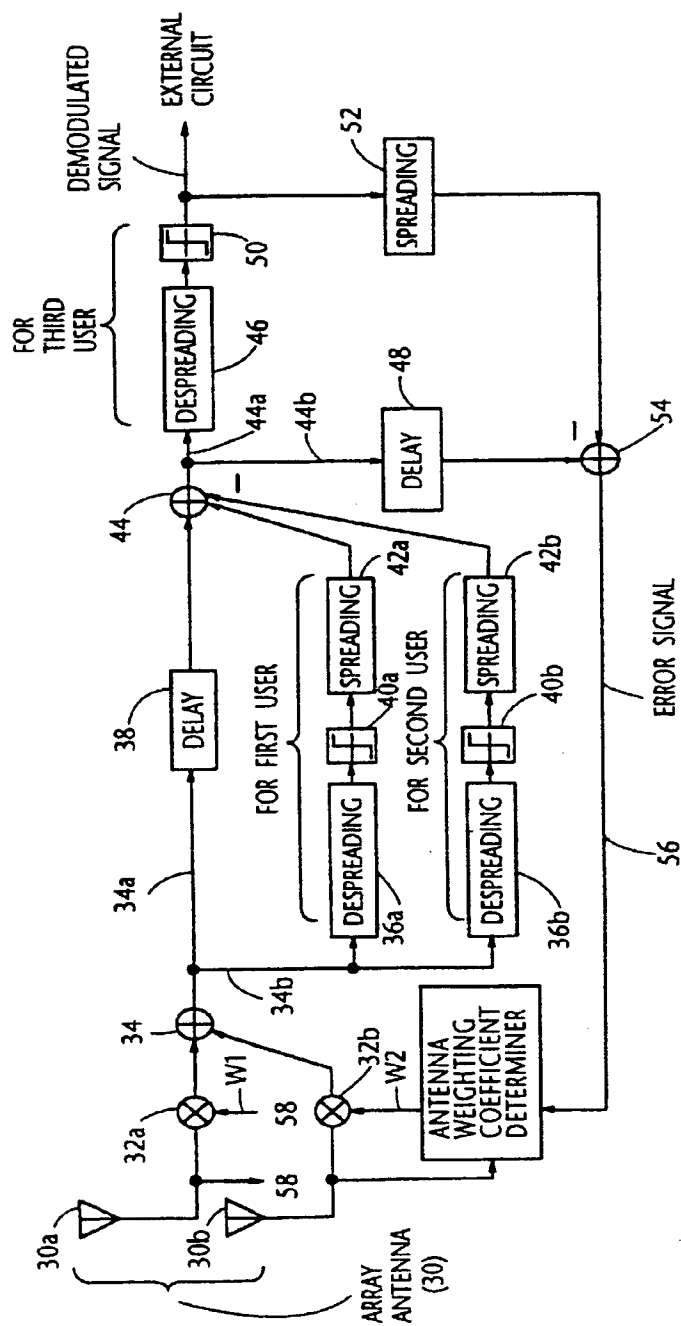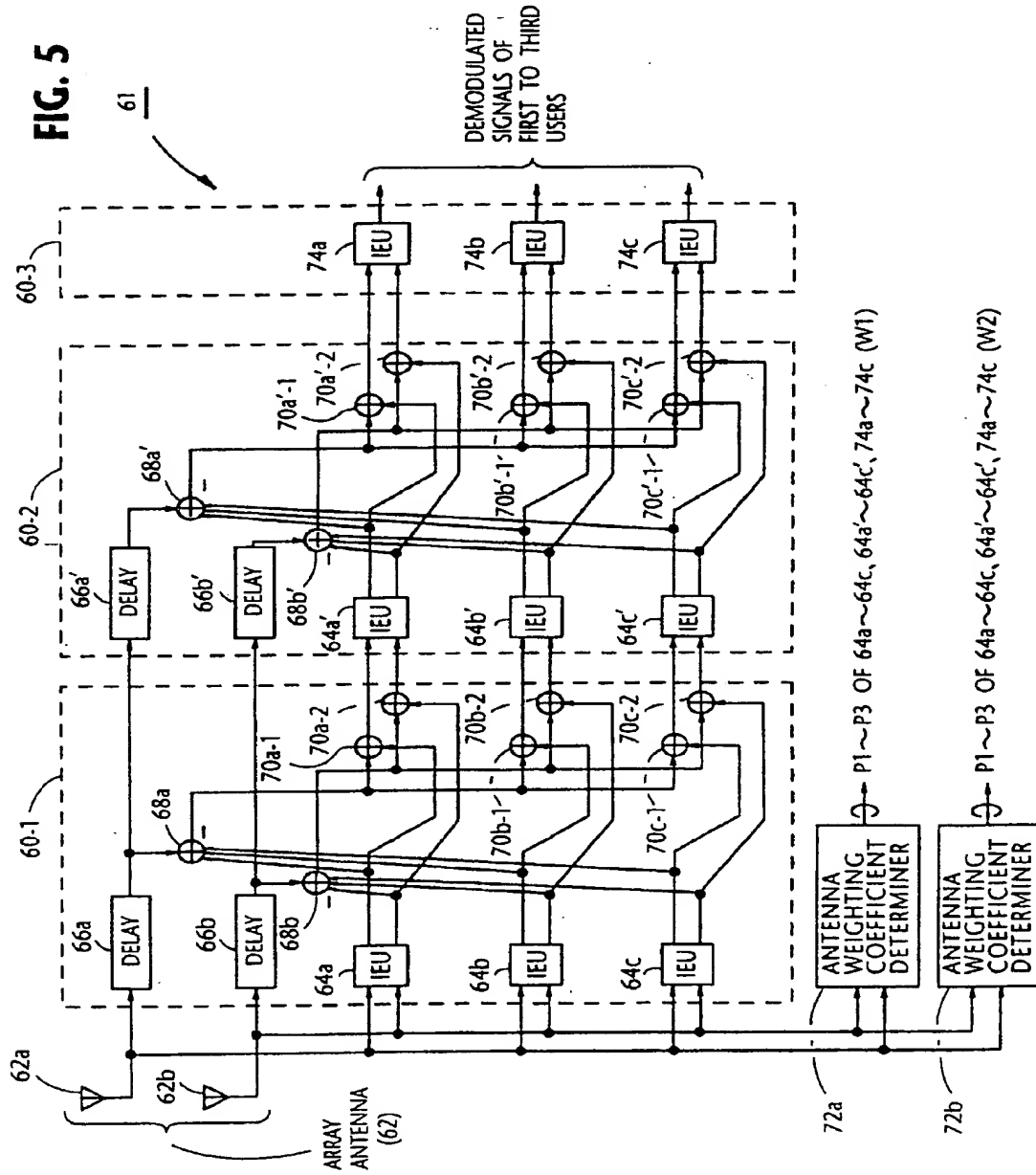
FIG. 6
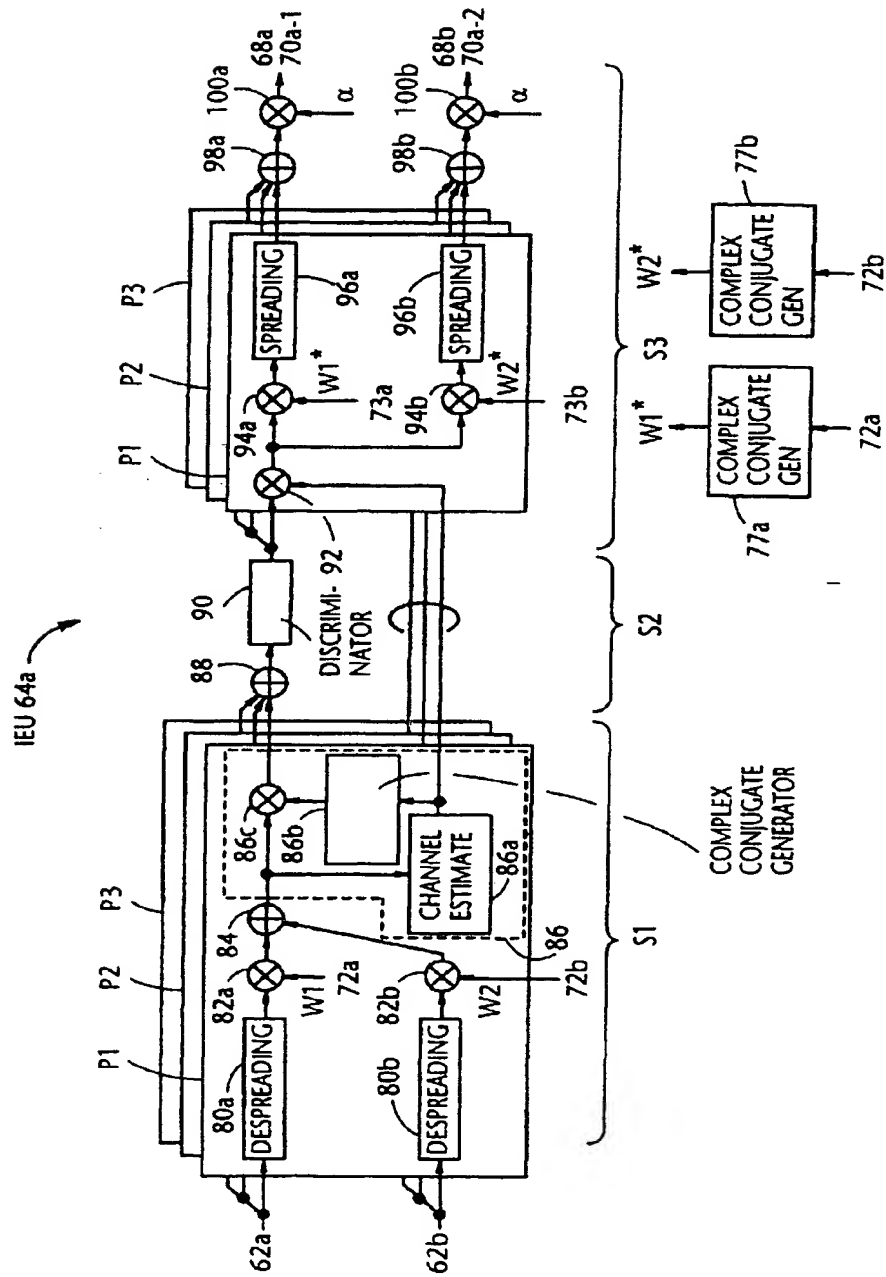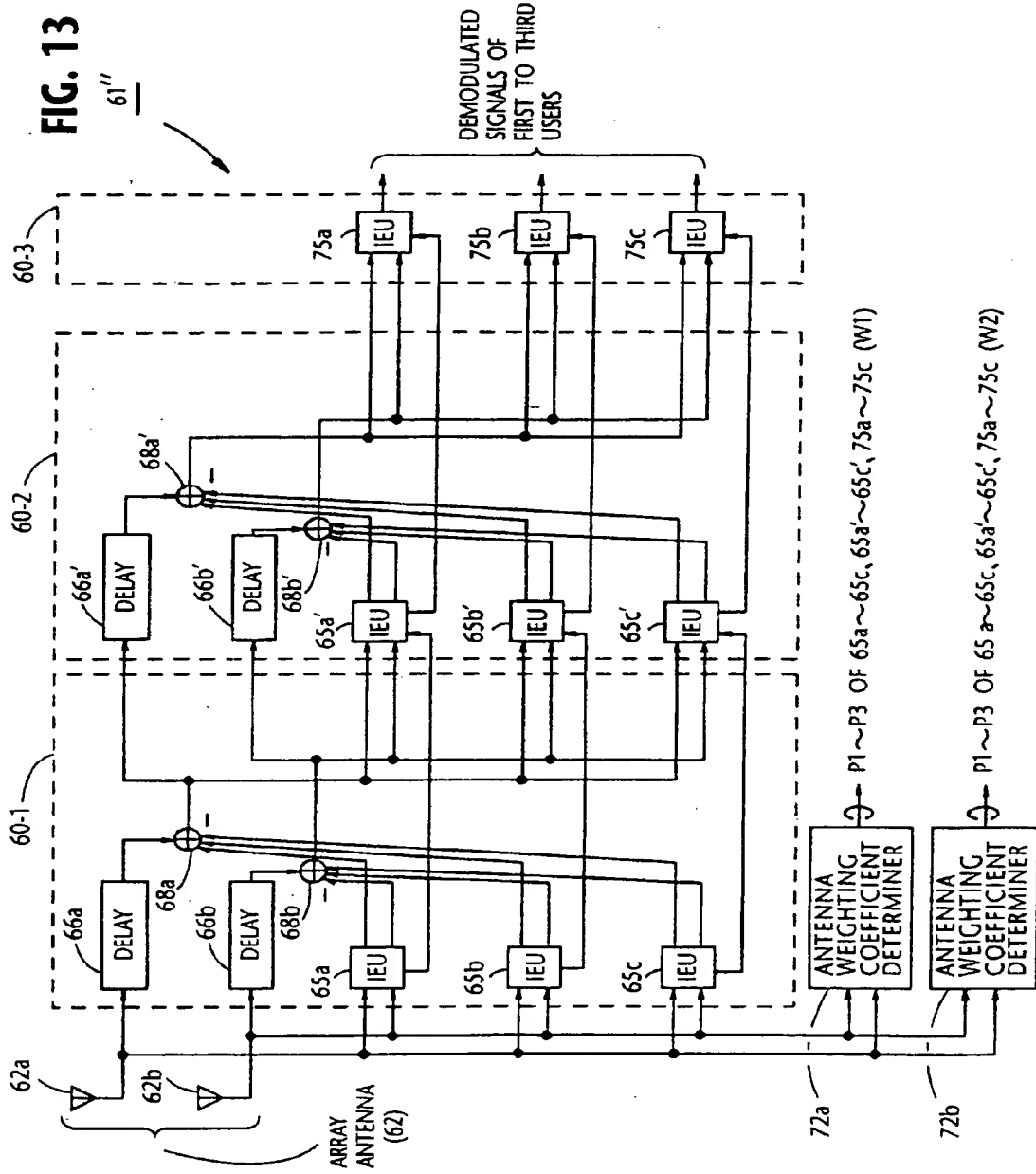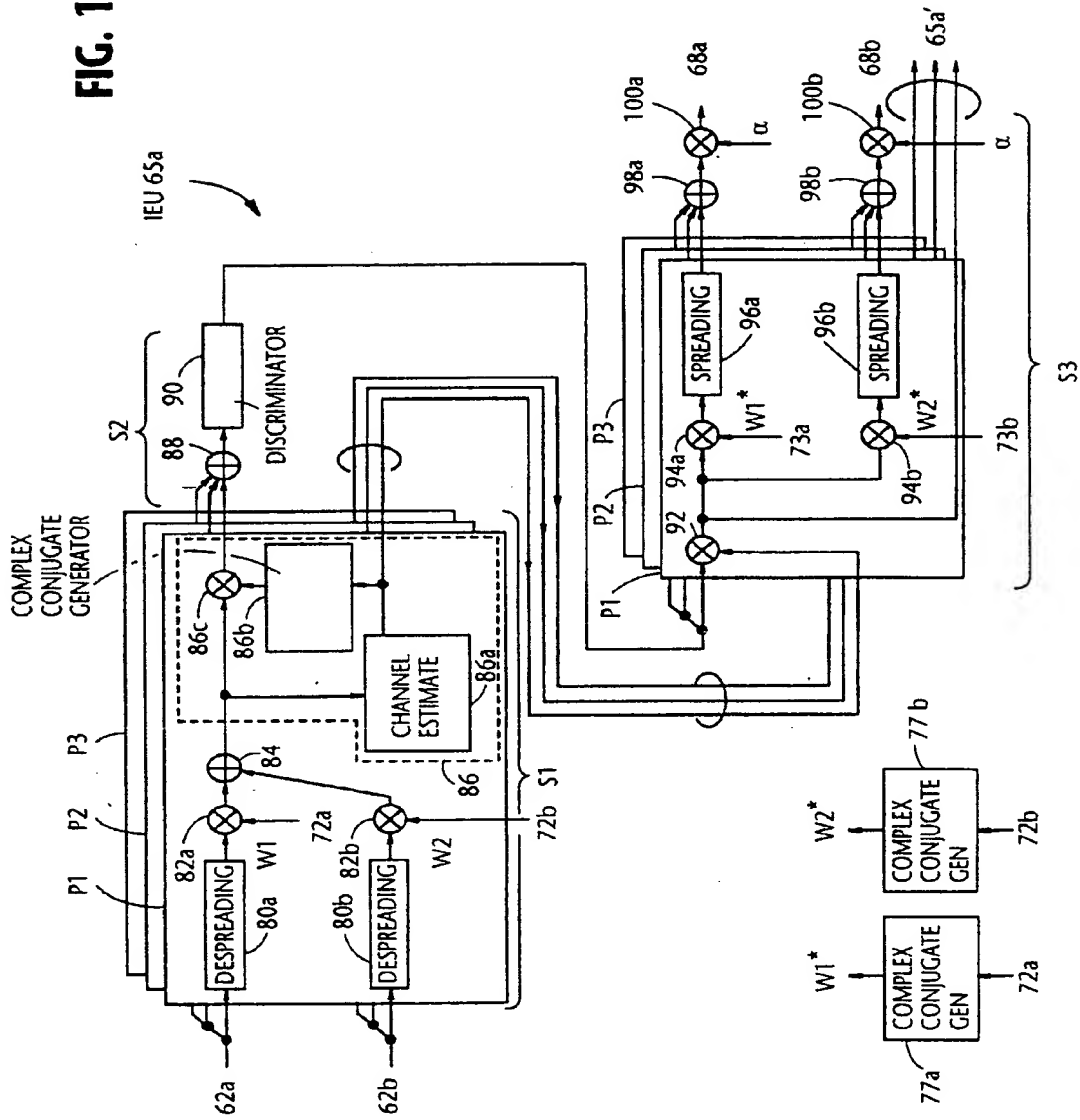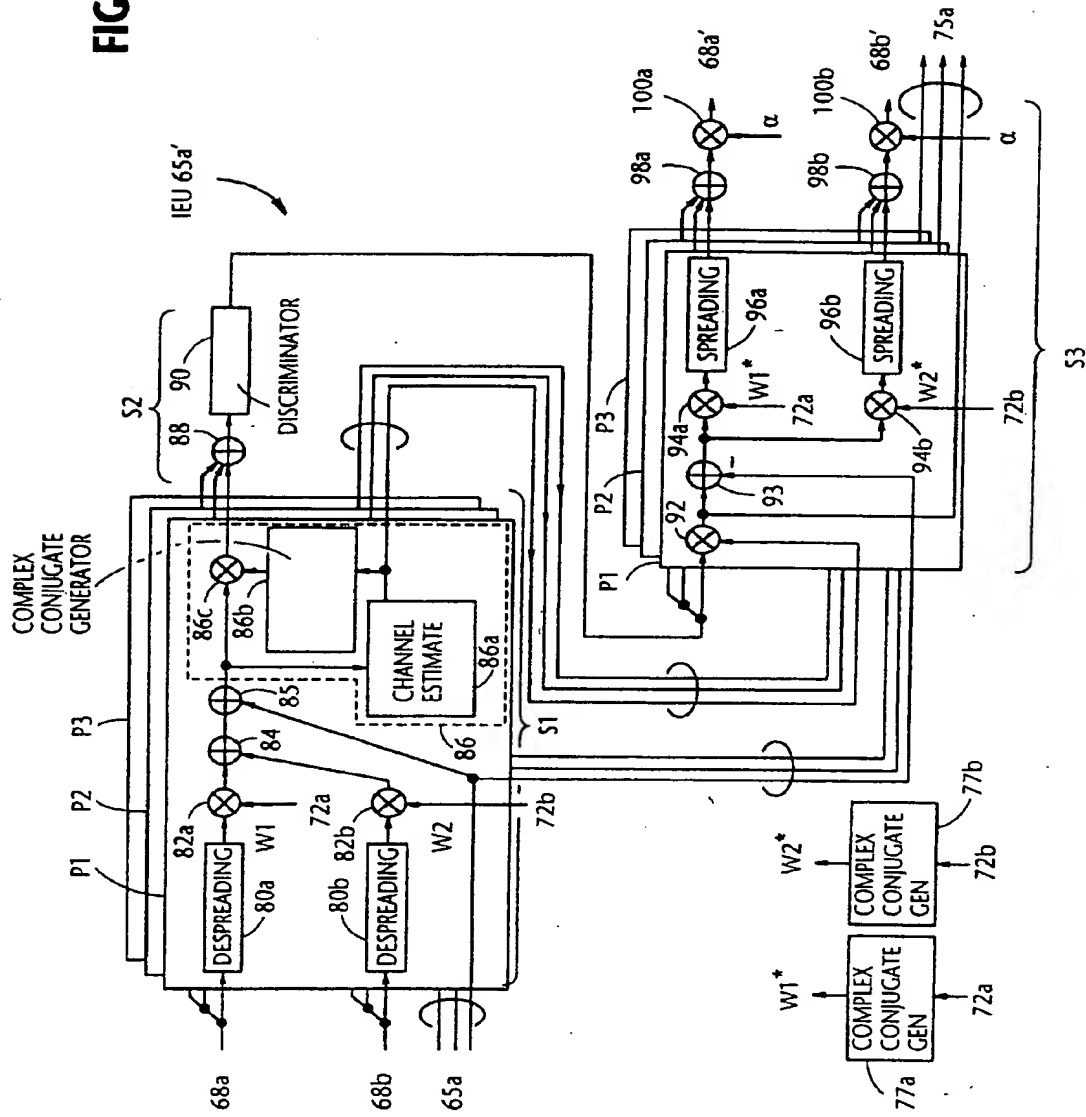
FIG. 7
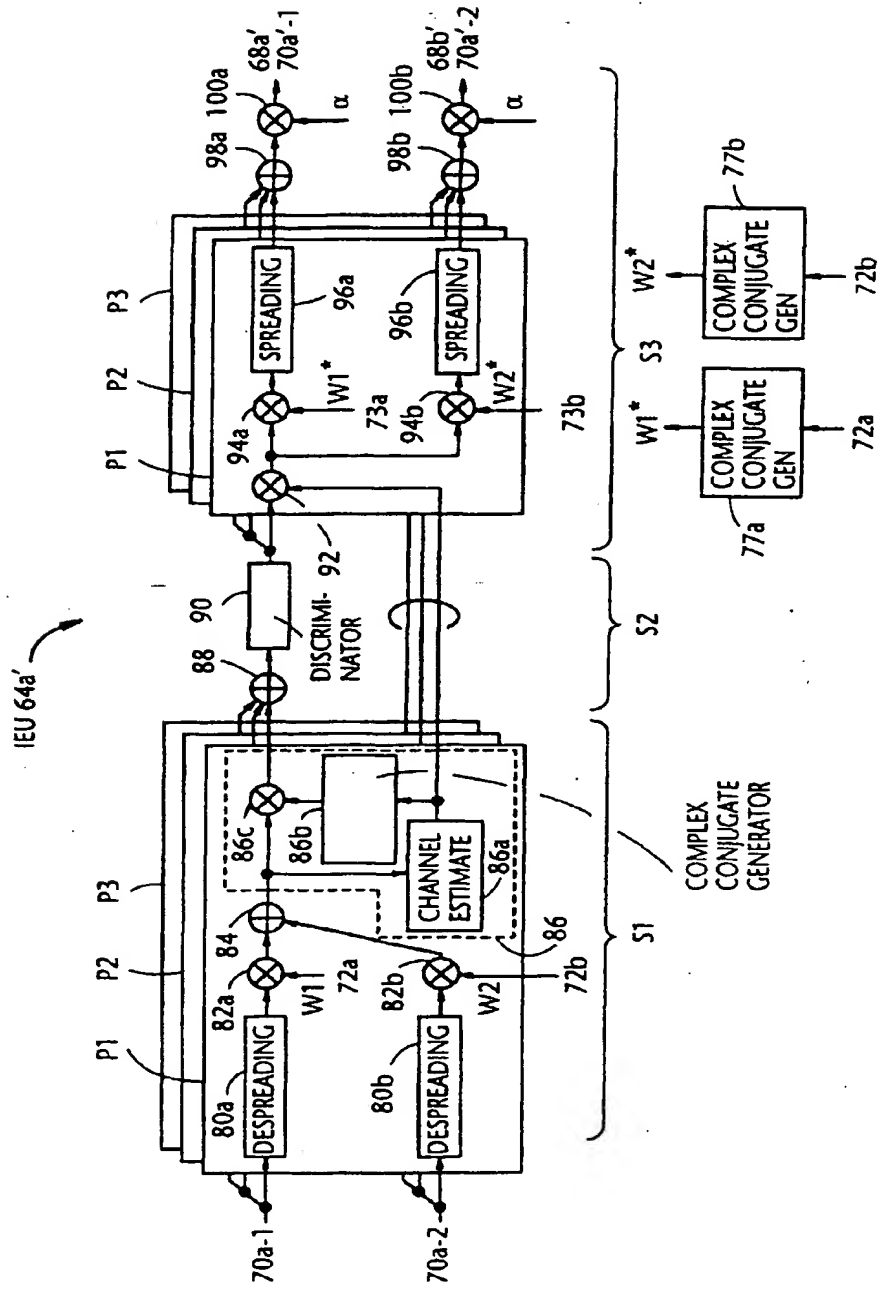
FIG. 8
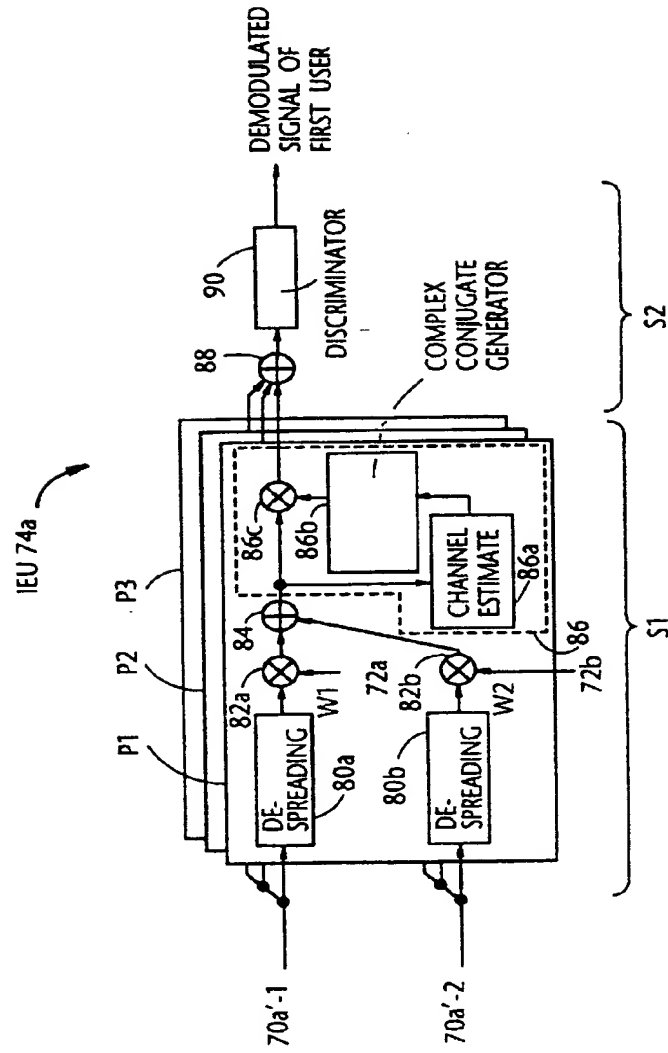
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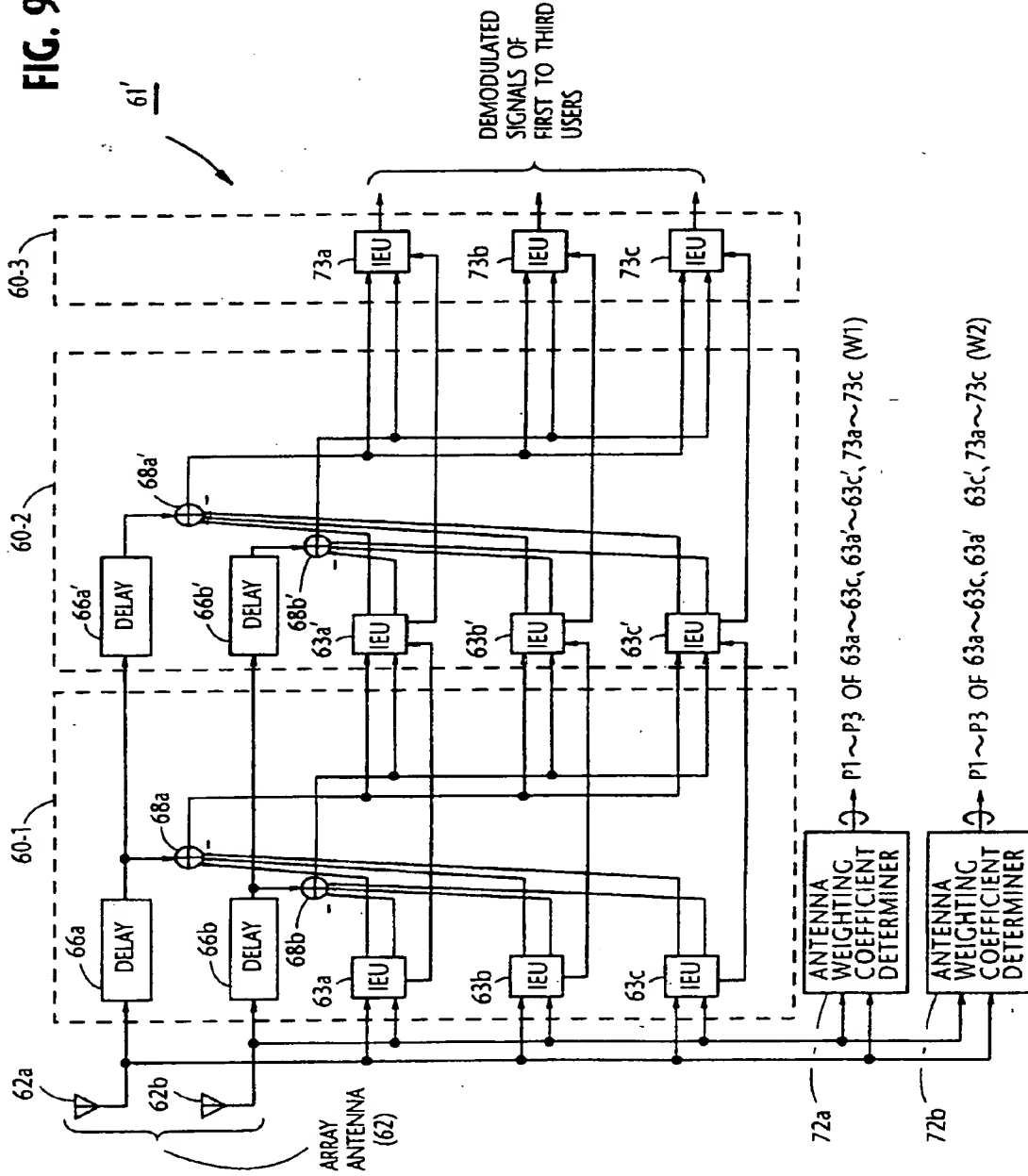
FIG. 10

FIG. 11

FIG. 12

FIG. 13
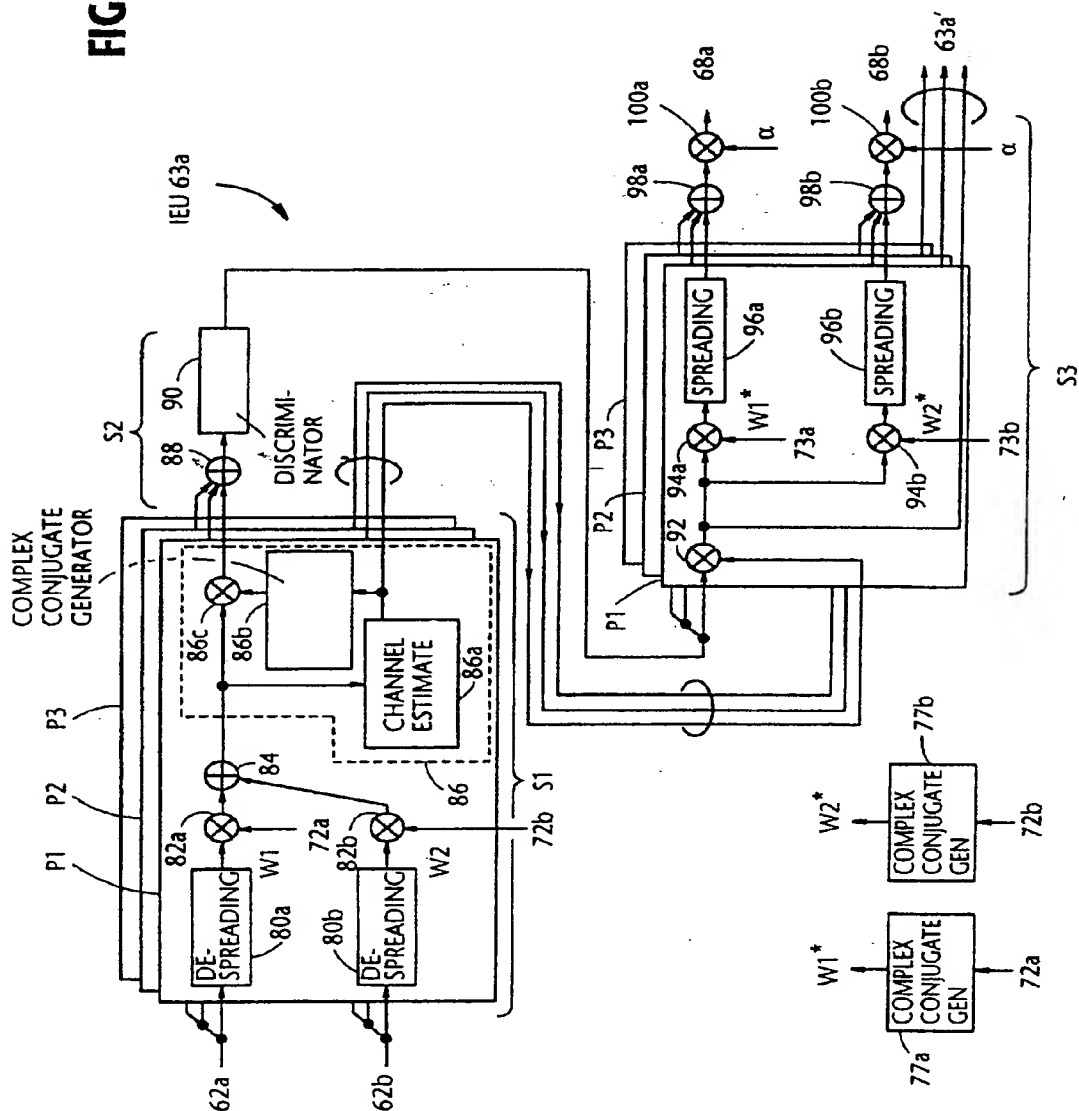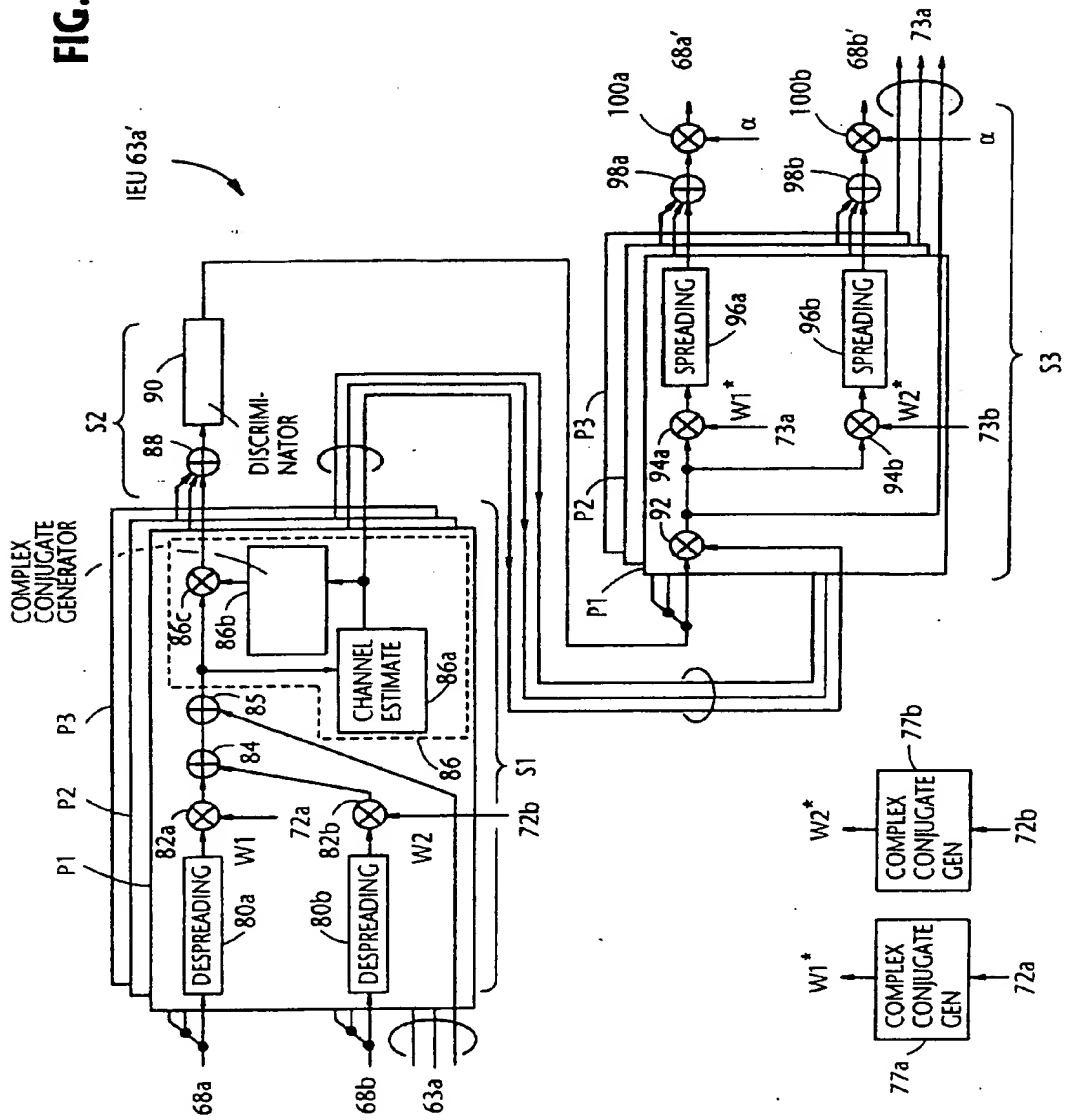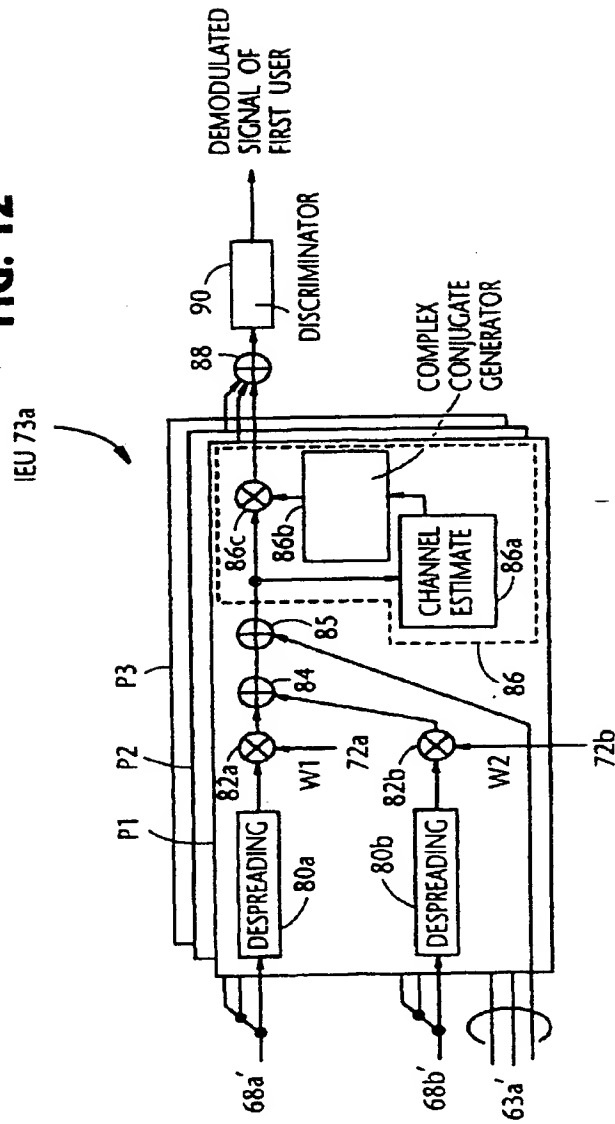
FIG. 14

FIG. 15

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